9306

MSI UP/DOWN BCD COUNTER

A FAIRCHILD COMPATIBLE CURRENT SINKING LOGIC PRODUCT

GENERAL DESCRIPTION — The 9306 is a high speed synchronous 8421 BCD up/down decade counter. It is a synchronously presetable, multifunctional MSI building block useful in a large number of counting, digital integration, and conversion applications. Seven decades of synchronous operation are obtainable with no external gating packages required through an internal carry look-ahead counting technique.

FEATURES:

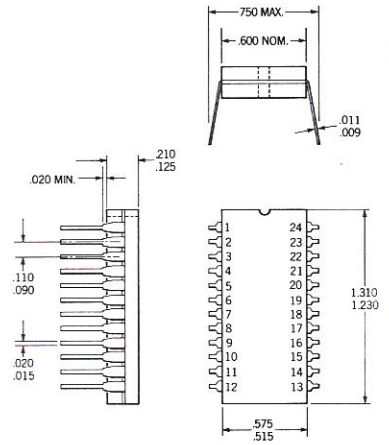
- **SYNCHRONOUS COUNTING AND PARALLEL ENTRY**
- **DECODED TERMINAL COUNT**
- **BUILT-IN CARRY/BORROW CIRCUITRY**
- **TYPICAL POWER DISSIPATION OF 350 mW**
- **THE INPUT/OUTPUT CHARACTERISTICS PROVIDE EASY INTERFACING WITH FAIRCHILD DTμL, LPDTμL, AND TTμL FAMILIES (CCSL).**
- **ALL CERAMIC HERMETIC 24 PIN DUAL IN-LINE PACKAGE**
- **INPUT DIODE CLAMPING**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

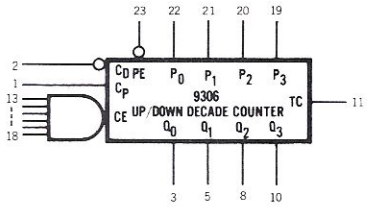
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7 V
Voltage Applied to Outputs for high output state	−0.5 V to V_{CC} value
Input Voltage (D.C.)	−0.5 V to +5.5 V

ORDER INFORMATION — Specify U6N9306XXX for 24-pin Dual In-Line package where XXX is 51X for the −55°C to +125°C temperature range, or 59X for the 0°C to 75°C temperature range.

PHYSICAL DIMENSIONS



LOGIC DIAGRAM



V_{CC} — Pin 24
Gnd — Pin 12

313 FAIRCHILD DRIVE, MOUNTAIN VIEW, CALIFORNIA, (415) 962-5011, TWX: 910-379-6435

FAIRCHILD SEMICONDUCTOR
A DIVISION OF FAIRCHILD CAMERA AND INSTRUMENT CORPORATION

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MANUFACTURED UNDER ONE OR MORE OF THE FOLLOWING U. S. PATENTS: 2981877, 3015048, 3025589, 3064167, 3108359, 3117260; OTHER PATENTS PENDING.

FUNCTIONAL DESCRIPTION — A clock buffer and inverter drives the four clocked RS master-slave flip flops in parallel, so that synchronous operation is obtained. When the clock input (CP) is low, the slave is steady, but data can enter the master via the R and the S inputs. During the low to high transition of CP, first the data inputs (R and S) are inhibited, so that a later change in the input data will not affect the master; secondly, the now trapped information in the master is transferred to the slave and is reflected at the outputs. When the transfer is completed both the master and the slave are steady as long as the clock input remains high, and regardless of the logic state at any other input to the device. During the high to low transition of the clock input, first the transfer path from master to slave are inhibited, leaving the slave steady in its present state, secondly, the data inputs (R and S) are enabled so that new data can enter the master. As a result of this synchronous operation higher clock frequency is possible and much less external logic is required in most applications. Mode selection is accomplished as shown in the table below. However, several restrictions are placed on the manner of selection. First, the transition of CE from high to low or of PE from low to high may only be done when CP is high. Second, any change of CD must be done only when CP is high. The remaining transitions may be made by following the setup and release times specified under "Switching Characteristics."

MODE SELECTION SCHEME

PE	CD	CE	Mode
0	0	0	presetting
0	0	1	presetting
0	1	0	presetting
0	1	1	presetting
1	1	1	count up
1	0	1	count down
1	1	0	no change
1	0	0	no change

Note: $CE = CE_0 \cdot CE_1 \cdot CE_2 \cdot CE_3 \cdot CE_4 \cdot CE_5$

LOADING RULES
(1 U.L. = 1 TTμL input gate load)

INPUT	FAN IN
CD, CE_0, CE_1, CE_2,	1 Unit Load
CE_3, CE_4, CE_5	1 Unit Load
CP, PE	2 Unit Loads
P_0, P_1, P_2, P_3	⅔ Unit Load
OUTPUT	**FAN OUT**
Q_0, Q_1, Q_2, Q_3, TC	6 Unit Loads

ELECTRICAL CHARACTERISTICS ($T_A = -55°C$ to $+125°C$, $V_{CC} = 5.0\ V \pm 10\%$)

SYMBOL	CHARACTERISTICS	LIMITS −55°C MIN.	LIMITS −55°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +125°C MIN.	LIMITS +125°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	2.7		2.4		Volts	$V_{CC} = 4.5\ V$, $I_{OH} = -0.36\ mA$
V_{OL}	Output Low Voltage		0.4		0.2	0.4		0.4	Volts	$V_{CC} = 5.5\ V$, $I_{OL} = 9.6\ mA$ $V_{CC} = 4.5\ V$, $I_{OL} = 7.44\ mA$
V_{IH}	Input High Voltage	2.0		1.7			1.4		Volts	Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.8			0.9		0.8	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current E_0, E_1, E_2, E_3, E_4, E_5, CD		−1.6		−1.0	−1.6		−1.6	mA	
$2\ I_F$	Input Load Current CP, PE		−3.2		−2.0	−3.2		−3.2	mA	$V_{CC} = 5.5\ V$ $V_F = 0.4\ V$
$⅔ I_F$	Input Load Current P_0, P_1, P_2, P_3		−1.07		−.7	−1.07		−1.07	mA	
I_R	Input Leakage Current E_0, E_1, E_2, E_3, E_4, E_5, CD		60		10	60		60	μA	
$2\ I_R$	Input Leakage Current CP, PE		120		20	120		120	μA	$V_{CC} = 5.5\ V$ $V_R = 4.5\ V$
$⅔ I_R$	Input Leakage Current P_0, P_1, P_2, P_3		40		7	40		40	μA	

ELECTRICAL CHARACTERISTICS ($T_A = 0°C$ to $+75°C$, $V_{CC} = 5.0\ V \pm 5\%$)

SYMBOL	CHARACTERISTICS	LIMITS 0°C MIN.	LIMITS 0°C MAX.	LIMITS +25°C MIN.	LIMITS +25°C TYP.	LIMITS +25°C MAX.	LIMITS +75°C MIN.	LIMITS +75°C MAX.	UNITS	CONDITIONS & COMMENTS
V_{OH}	Output High Voltage	2.4		2.4	3.0		2.4		Volts	$V_{CC} = 4.75\ V$, $I_{OH} = -0.36\ mA$
V_{OL}	Output Low Voltage		0.45		0.2	0.45		0.45	Volts	$V_{CC} = 5.25\ V$, $I_{OL} = 9.6\ mA$
V_{IH}	Input High Voltage	1.9		1.8			1.6		Volts	$V_{CC} = 4.75\ V$, $I_{OL} = 8.5\ mA$ Guaranteed input high threshold for all inputs
V_{IL}	Input Low Voltage		0.85			0.85		0.85	Volts	Guaranteed input low threshold for all inputs
I_F	Input Load Current $E_0, E_1, E_2, E_3, E_4, E_5, CD$		−1.6		−1.0	−1.6		−1.6	mA	
$2\ I_F$	Input Load Current CP, PE		−3.2		−2.0	−3.2		−3.2	mA	$V_{CC} = 5.25\ V$ $V_F = 0.4\ V$
$⅔ I_F$	Input Load Current P_0, P_1, P_2, P_3		−1.07		−.7	−1.07		−1.07	mA	
I_R	Input Leakage Current $E_0, E_1, E_2, E_3, E_4, E_5, CD$		60		10	60		60	μA	
$2\ I_R$	Input Leakage Current CP, PE		120		20	120		120	μA	$V_{CC} = 5.25\ V$ $V_R = 4.5\ V$
$⅔ I_R$	Input Leakage Current P_0, P_1, P_2, P_3		40		7	40		40	μA	

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS & COMMENTS
t_{pd+} (Q)	Turn-Off Delay		20		ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ (Fig. 1)
t_{pd-} (Q)	Turn-On Delay		20		ns	
t_{pd+} (TC)	Turn-Off Delay for TC		40		ns	
t_{pd-} (TC)	Turn-On Delay for TC		30		ns	
t_s (CE)	Set-Up Time for CE		25		ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ (Fig. 2)
t_r (CE)	Release Time for CE		25		ns	
t_s	Set-Up Time for Data		15		ns	$V_{CC} = 5.0\ V$ $C_L = 15\ pF$ (Fig. 3)
t_r	Release Time for Data		15		ns	
t_s (PE)	Set-Up Time for PE		20		ns	
t_r (PE)	Release Time for PE		20		ns	

SET-UP TIME: t_s is defined as the minimum time required for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) to respond.

RELEASE TIME: t_r is defined as the maximum time allowed for the logic level to be present at the logic input prior to the clock transition from low to high in order for the flip-flop(s) not to respond.

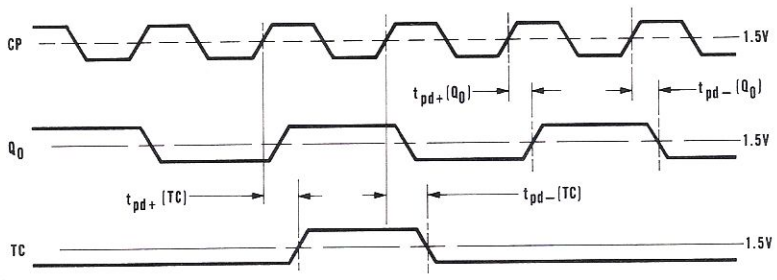

Fig. 1

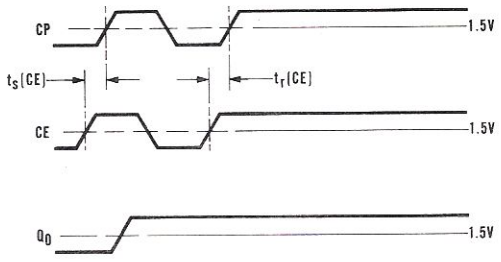

Fig. 2

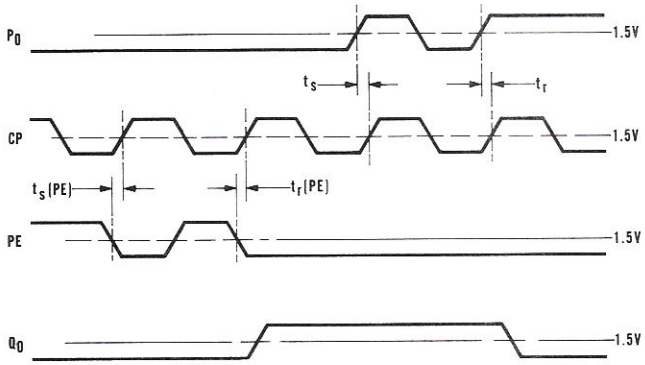

Fig. 3

APPLICATIONS

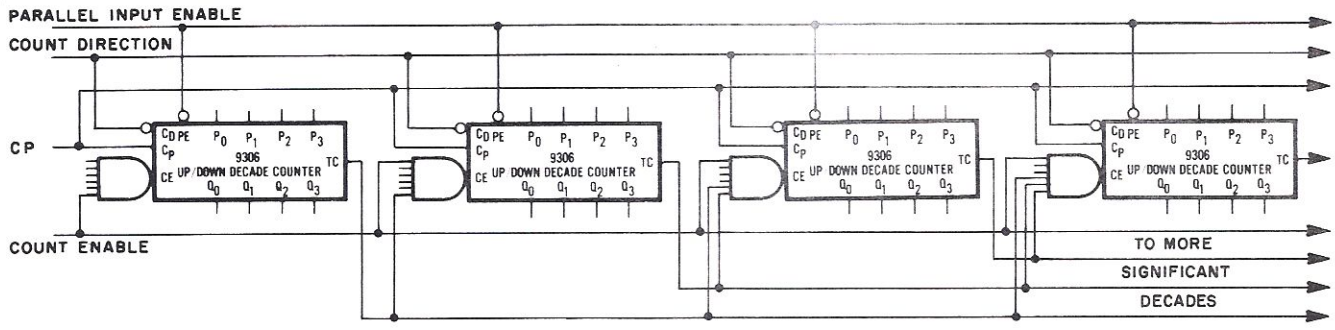

Fig. 4

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